

**Applicants hereby amend the paragraph on page 22, beginning on line 10 of the specification as follows:**

Referring to FIG. 2, a memory 100 having a plurality of addressable memory locations is connectable through the switching device 102 to one of the multiple buses 104-107 of a multibus architecture 110. Connections to the memory 100 include an address memory connection 114 and a data memory connection 116. The addresses for addressing internal memory locations of the memory 100, which may be transmitted through a separate address bus or through one of the buses 104-107, are applied to the address memory connection 114. The address information is supplied from the actively switched bus 104. It is also possible to have addresses supplied through the bus 104 in the form of a programming bus such that the switching device 102 implements switching to the programming bus 104 routinely or upon completion of a memory access. To implement a data access, the switch-over to the required additional bus 105-107 is effected as required.